

2025 Oct. 17 (Fri) - AI & Semiconductor Strategic Innovation



Dr. Patrick Cogez

PM 02:10 - 02:40

歐盟微電子研發補助前景以及產業協會扮演的角色

The European microelectronics funding landscape and the role of industrial associations in its governance and shape

Technical Director, 歐盟奈米電子研發產業協會 (AENEAS)



**The European microelectronics funding landscape
and the role of industrial associations in its governance and
shape**

Patrick Cogez, Technical Director

The 26th International Conference on Industrial Technology Innovation

17/10/2025



Presentation outline

- What is AENEAS ?
- AENEAS in the European Funding Landscape
 - Chips Joint Undertaking
 - EUREKA Xecs Programme
- The ECS Strategic Research and Innovation Agenda
 - Structure and elaboration
- Other AENEAS activities relevant for EU-Taiwan cooperation
 - International Cooperation on Semiconductors
 - Tackling the talent gap



AENEAS association

Visit <https://aeneas-office.org/>

AENEAS is a **not-for-profit Industrial Association** representing its members in the **Electronic Components and Systems (ECS)** value chain:

Large industries, Small and Medium Enterprises, Research institutes, universities and associated org.

AENEAS aims at:

- ☞ Fostering **R&D&I**
- ☞ Creating an effective funding landscape

Supporting the Sustainable Digital transition of Europe:

- ☞ To maintain a competitive position
- ☞ To support its societal goals

AENEAS initiates and implements actions that:

- ☞ Promote networking
- ☞ Encourage collaborative consortia work
- ☞ Facilitate access to funding support

AENEAS synergies and partnerships with other communities

- ☞ Agreement between **AENEAS, EPoSS & Inside** related to ECSEL, KDT and the Chips JU
- ☞ MoU with **SEMI Europe** since 2018
- ☞ MoU with **6G IA** since 2022
- ☞ MoU with **QuIC**, the Quantum Industry Consortium, since 2022
- ☞ Member of the **Alliance on Processors and Semiconductor Technologies**
- ☞ **ICOS** CSA on International Collaboration On Semiconductors, 2023-2025
- ☞ **European Chips Skills Academy**, ERASMUS+ project, 2023-2027, including a **Summer School**

AENEAS members are key industrial players

Jochen Hanebeck, CEO of Infineon, is AENEAS President



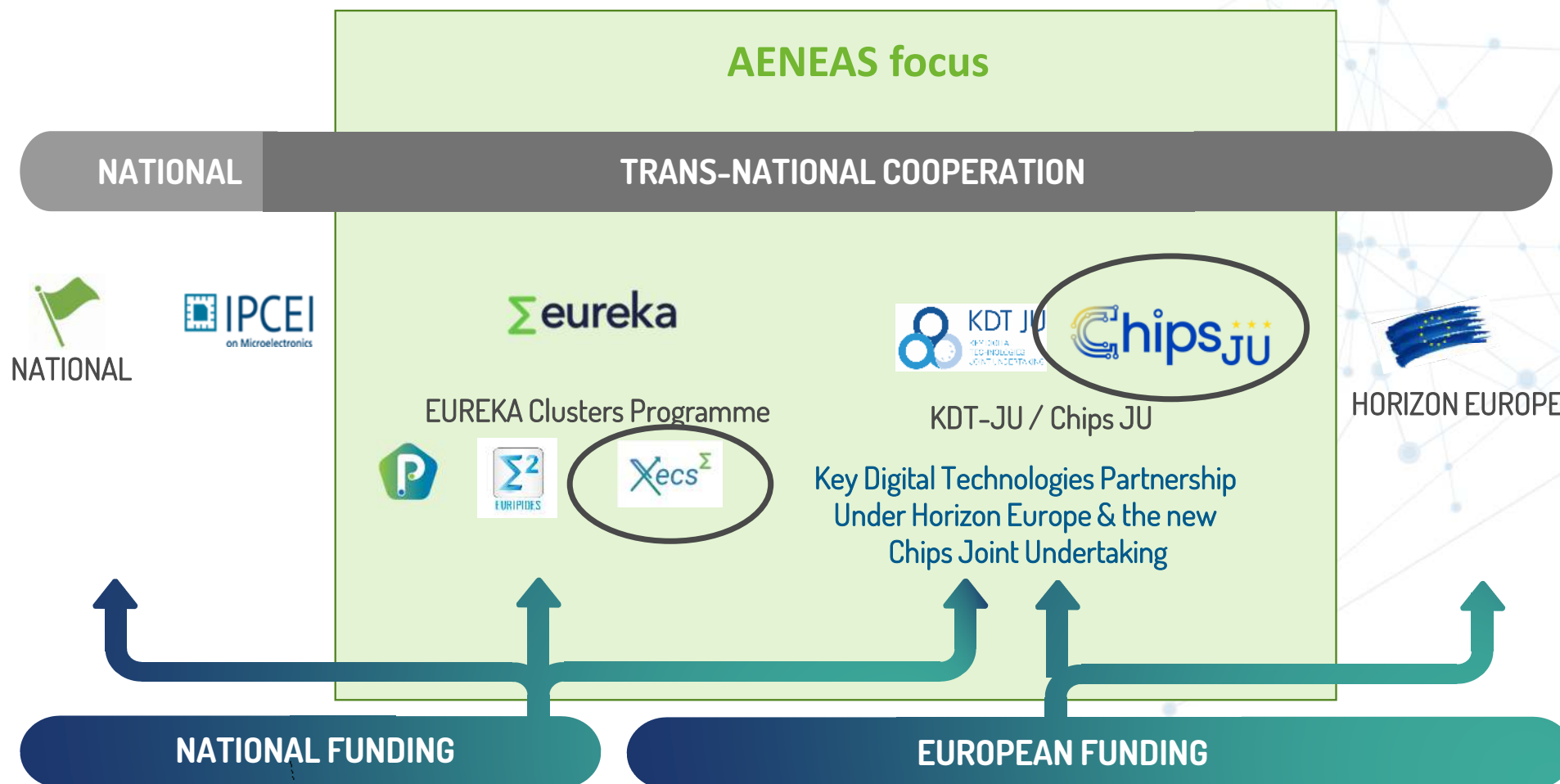
20 seats of the Supervisory Board:

- 4 SME (Chamber A)
- 4 RT0 (Chamber B)
- 12 Large Enterprises (chamber C)

570 members in June 2025:

49% SMEs, 24% RT0, 23% Corporate, 4% Associate

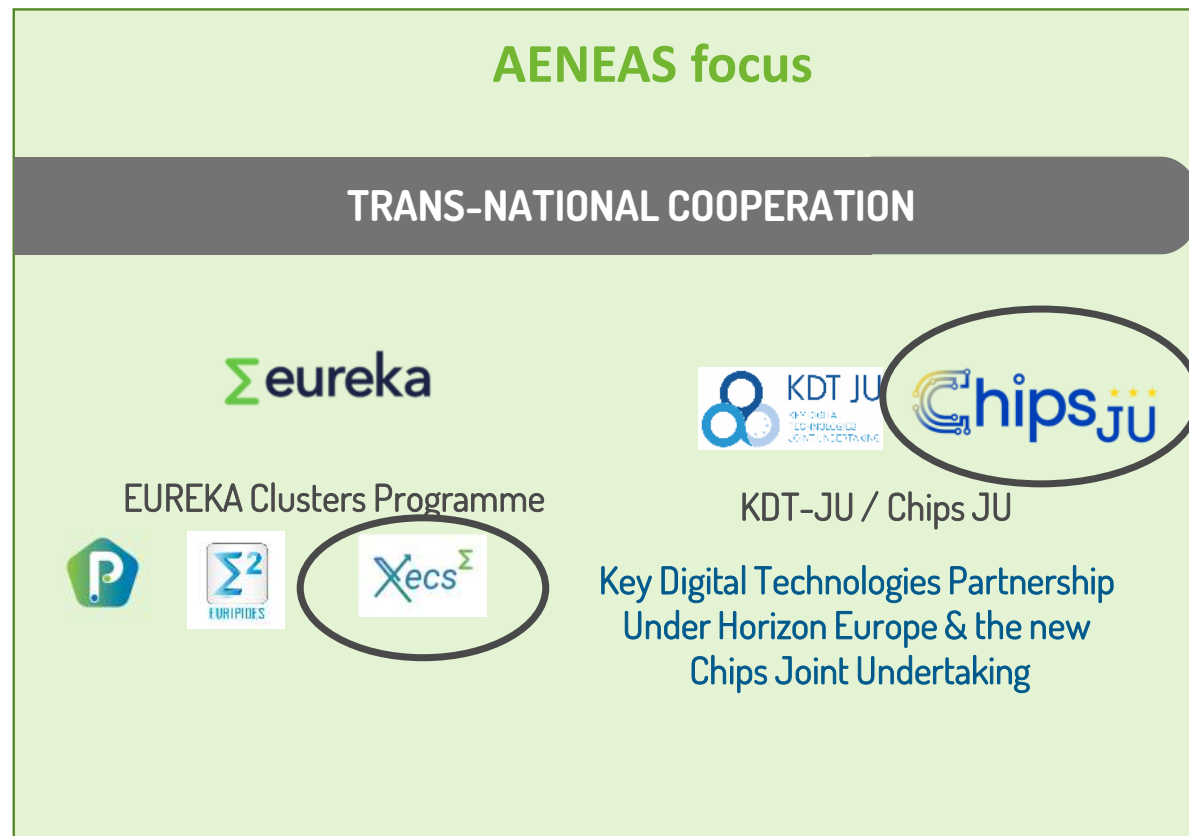
See <https://aeneas-office.org/>



AENEAS role in the ECS funding landscape

AENEAS operates Xecs: the Xecs Office is part of AENEAS:

- Launches the Calls
- Appoints technical experts to evaluate the proposals
- Organises funding decision with the Public Authorities
- Monitors the projects (reviews, reports, etc.) until their end
- Highlights impact after the project end



- **AENEAS represents Industry in the Chips JU:**
- Sits at the Governing Board, with EC & PS
- Holds voting rights
- Is part of the Private Members Board:
 1. Delivering the SRIA
 2. Contributing, and negotiating the contents of the Calls and budgets
 3. Organising EF ECS
- Pays for the Chips JU office (with the EC)

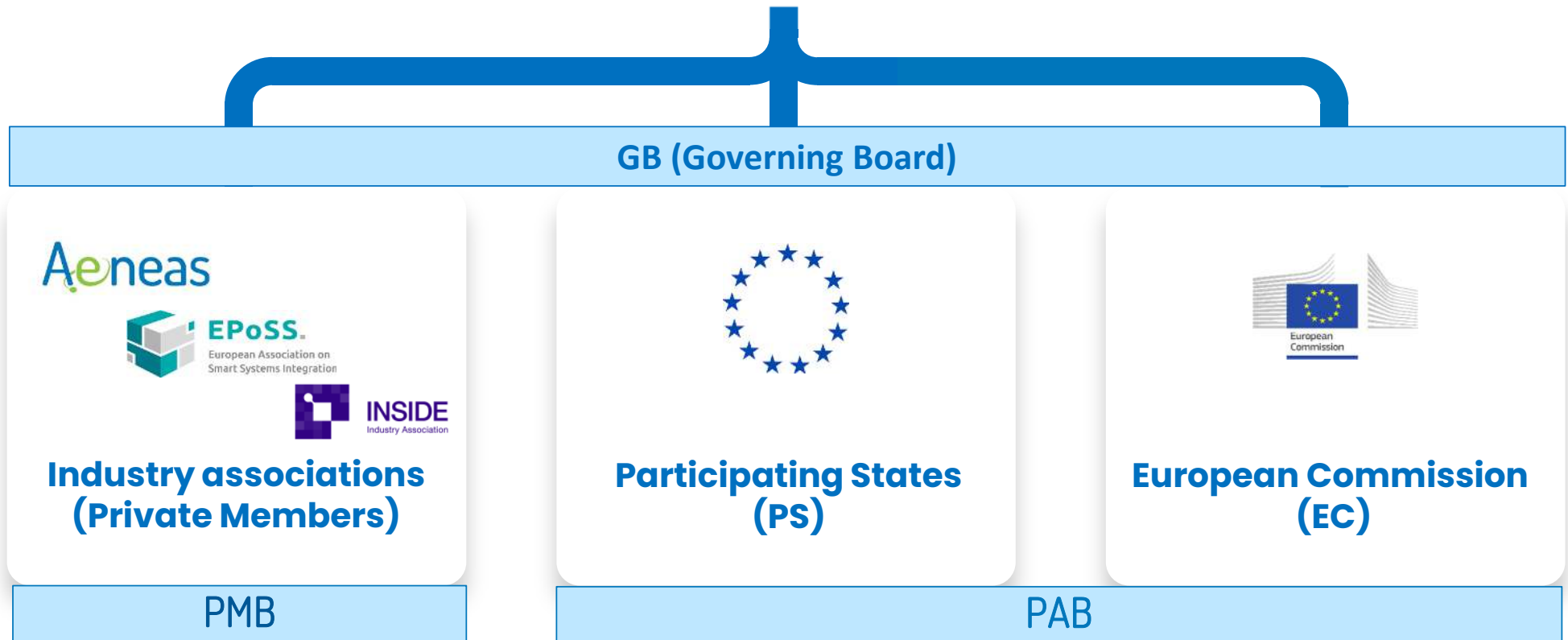


1 – The Chips JU

- The Chips JU is a **tri-partite** Public-Private Partnership between the European Commission and Participating States as public members and 3 Industry Associations AENEAS, EPoSS and INSIDE as private members
- **The Chips JU partnership** (2021-2027) is implemented as a **Joint Undertaking**, enlarging the preceding KDT JU with an extended scope and budget
- Total Chips JU programme size around **11B€**
- **It is made of 2 parts**, each operating with **yearly Calls**:
 1. **The regular R&I** programme, industry-driven, called **“ECS”** based on the ECS Strategic Research and Innovation Agenda, which may include Focus Topics (in continuation of KDT)
 2. **The Chips for Europe initiative**, as pillar 1 of the **EU Chips Act** (since 21 Sept 2023), deals with Pilot Lines, Design Platforms, Quantum chips and Competence Centers
- Selected projects receive funding from EC and Participating States

Aeneas

Chips JU governance

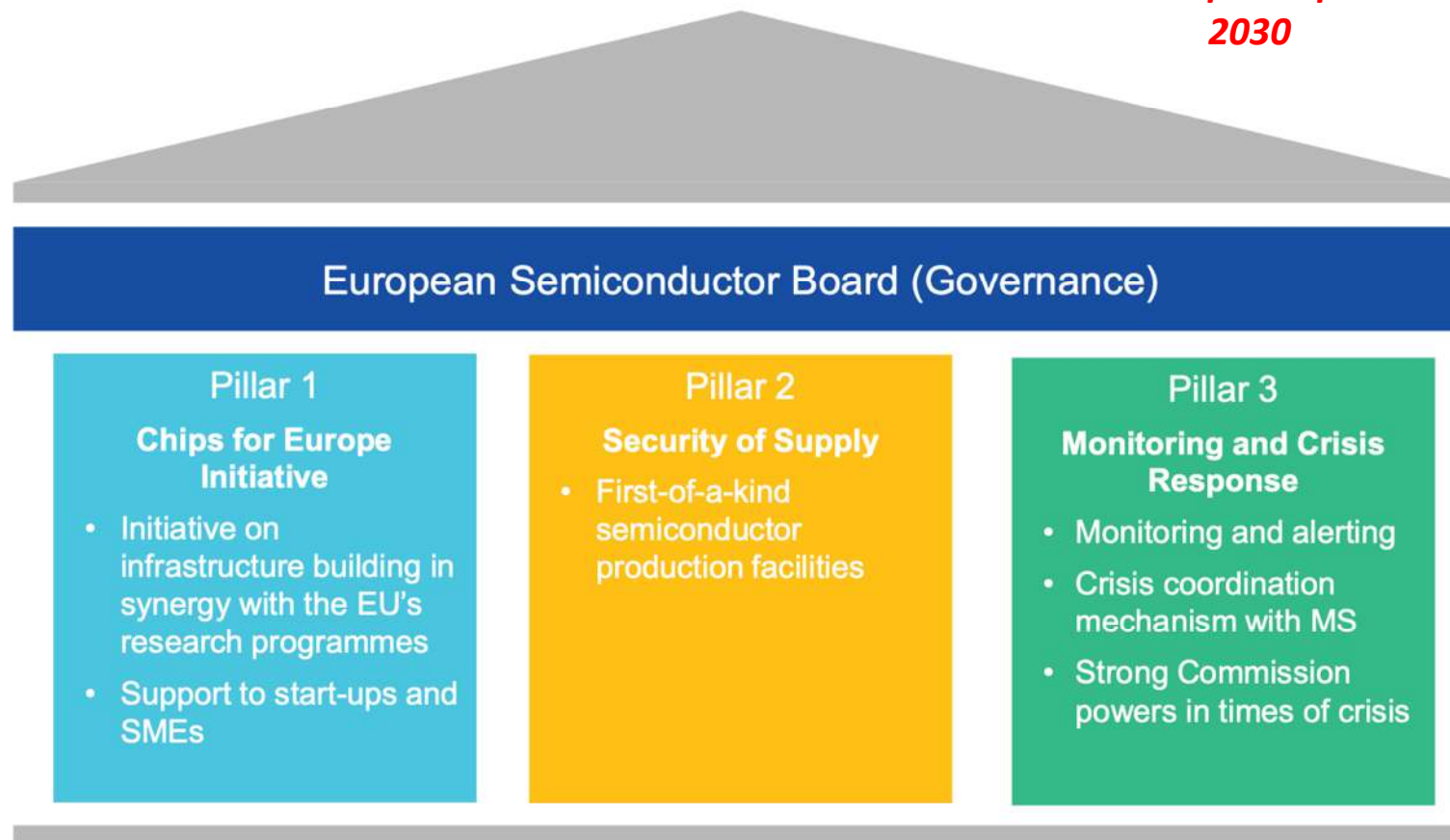


Chips Act package: European Commission

Three pillars of the Chips Act

***Comment: Chips Act > 43B€
public private investment up to
2030***

***Comment:
AENEAS
focusing on
Research &
Innovation
(R&I): Pillar 1
“Chips for
Europe
Initiative”. The
Chips Joint
Undertaking
replaces the
KDT Joint
Undertaking***





What is Σ eureka ?

The world's biggest public network for international cooperation in RD&I, present in over 45 countries.

Mainly European, but also including
Canada, Israel, Singapore, South Africa and South Korea

Intergovernmental organisation for
market-driven industrial RD&I
aiming to boost the productivity &
competitiveness of European
industries

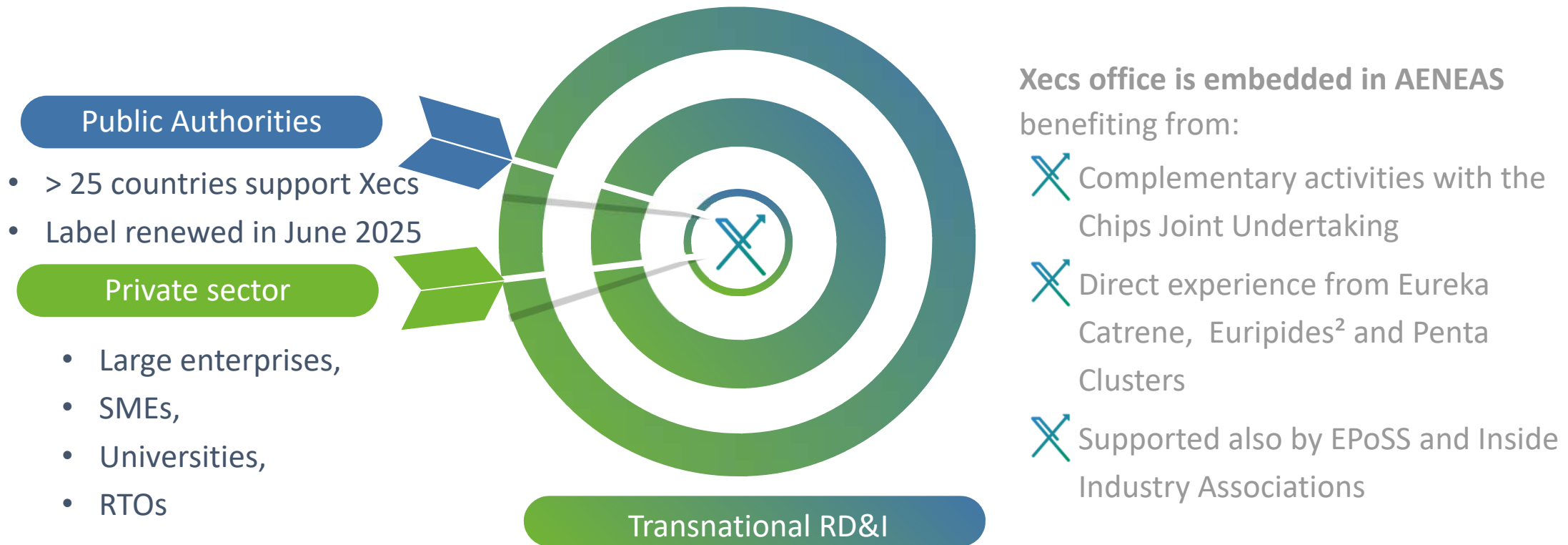


A transnational network facilitating
the coordination of national
priorities on innovation and
providing access to national funding

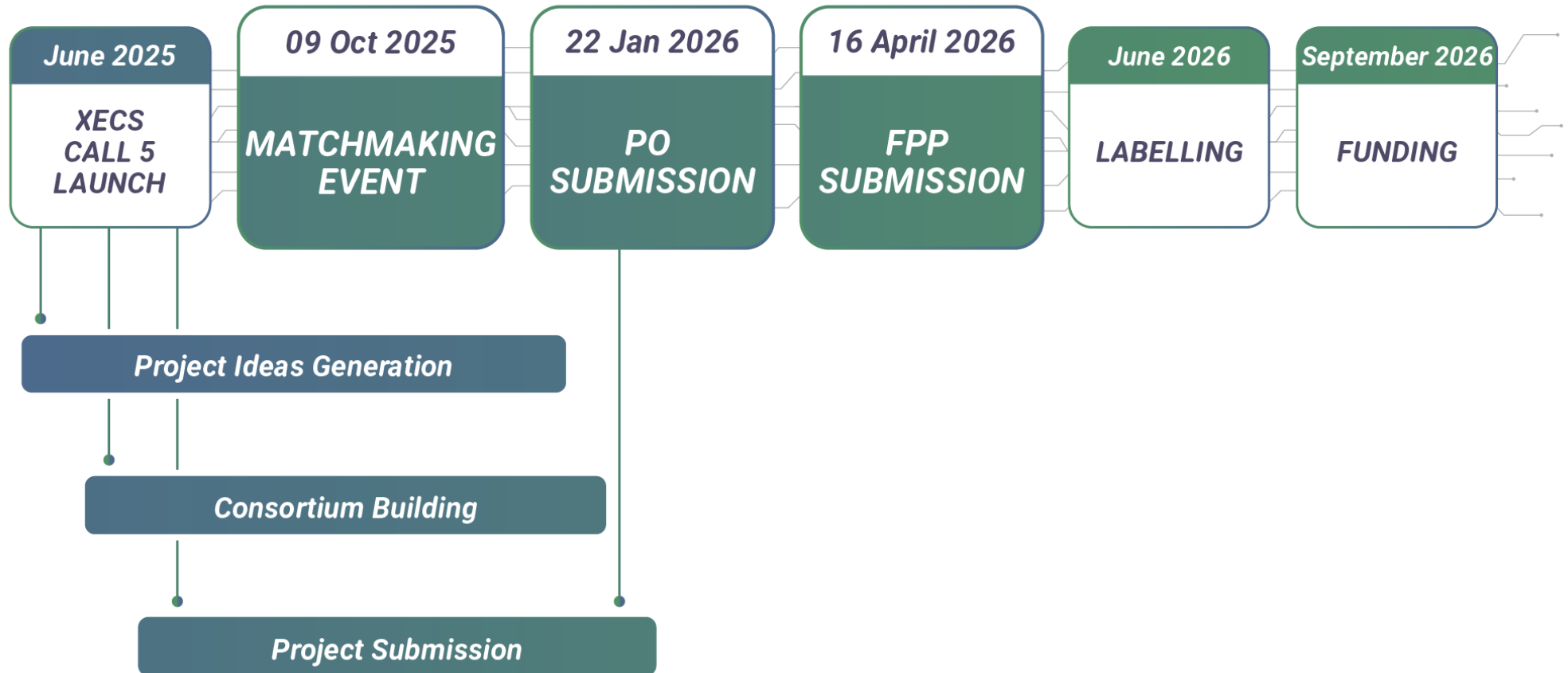
Xecs – A Eureka Cluster



supporting RD&I in the field of Electronic Components & Systems



Xecs Call 5 timeline





Eureka Cluster Xecs

- ✕ Open to all 47 Eureka countries and beyond
- ✕ National funding according to national rules

- ✕ Xecs is an additional EUREKA funding opportunity beyond GlobalStars
 - Provided that Taiwanese Public Authorities fund that programme
- ✕ Current call schedule (PO deadline January 22nd, 2026) well suited for Taiwanese partners to join now

- ✕ High flexibility in the course of the project e.g. for changes in the project
- ✕ Low administrative overhead, even SMEs can take the role of a project leader

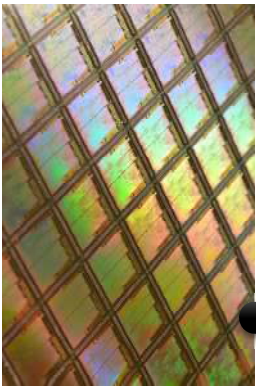
The ECS SRIA - Why ?

Align and coordinate research policies across Europe

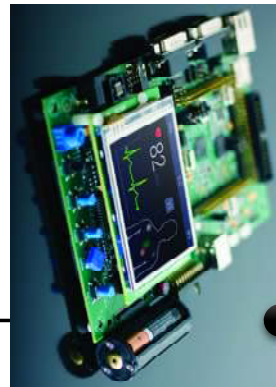


The ECS SRIA – What ?

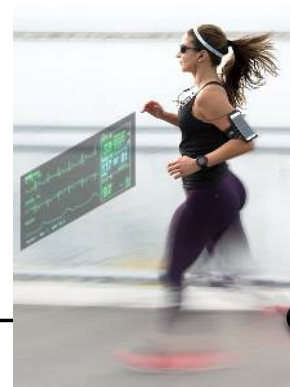
- Presenting **research topics** to be investigated over next 15 years
- To foster and accelerate our European **digital transformation** reflecting European values
- Covering the **whole value chain of Electronic Components & Systems (ECS)**



Materials, processes,
semiconductors, micro
& nano electronic
components, ...



Smart sensors,
integrated devices, edge
AI, embedded SW, ...

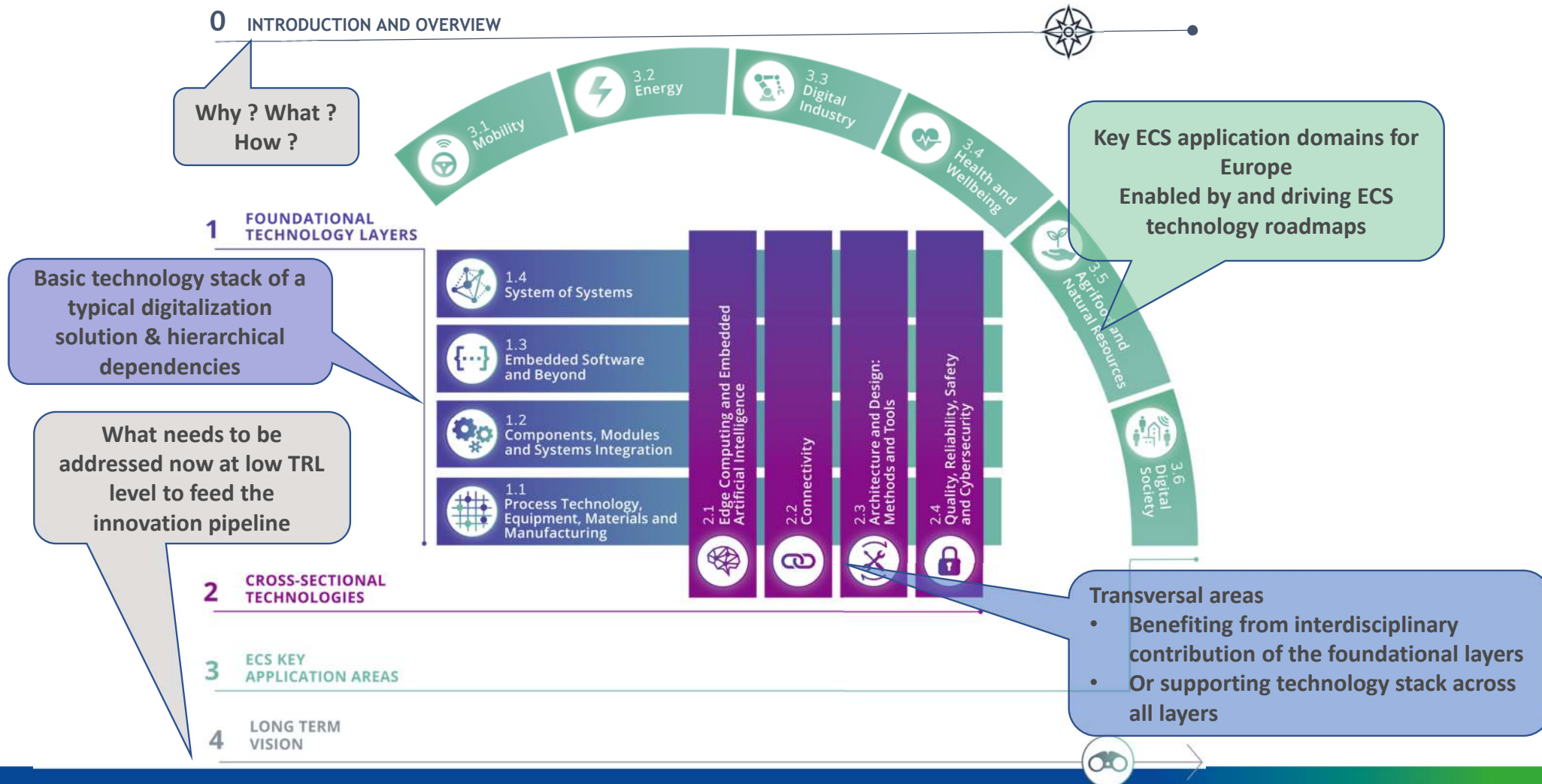


Systems and applications,
value creation, societal
goals, ...



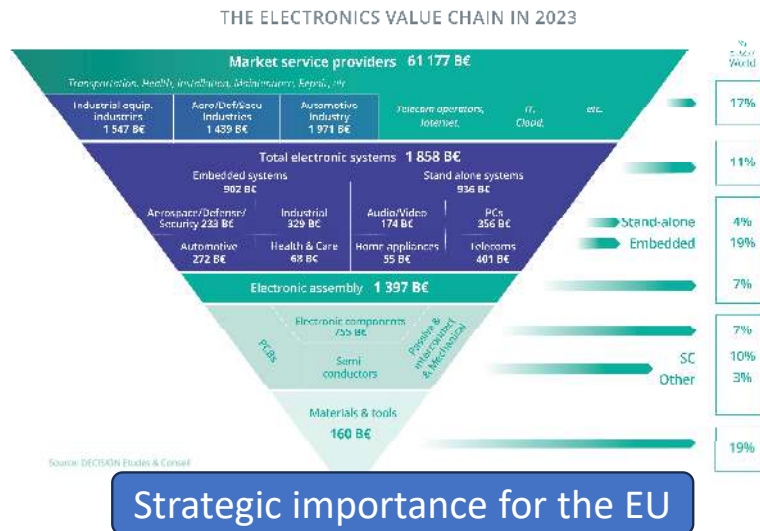
ECS engineering tools

ECS-SRIA structure

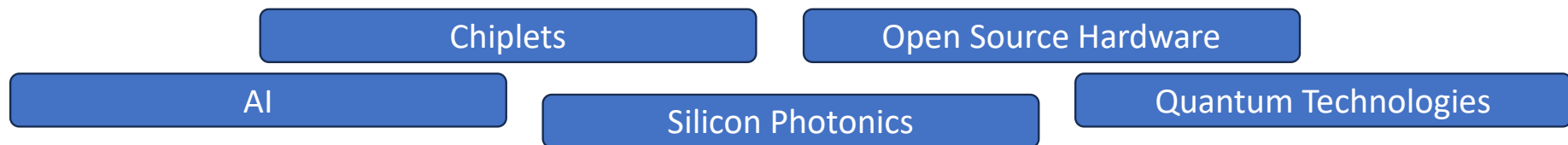


Ch. 0 - Strategic overview

- Why ECS matter



- What? SRIA content, including new and/or expanded cross-cutting themes



2005 ECS SRIA Edition available online



- Native indexing and analytics
- More advanced functionalities for:
 - Topics search
 - Selective reading
- Increased visibility and accessibility
 - Attract new talents and experts

- <https://ecssria.eu/>



Patrick Cogez
AENEAS
Chairman



Paolo Azzoni
INSIDE IA
Co-chairman



Matthias Küntzel
EPoSS
Co-chairman

The 2025 ECS SRIA – Who ?

Core Team

- Arco Krijgsman - ASML
- Christophe Wyon - CEA
- Jerker Delsing - Lulea University of Technology
- Jürgen Niehaus - SafeTRANS
- Patrick Pye - NXP
- Sven Rzepka - Fraunhofer
- Wolfgang Dettmann - Infineon Technologies AG

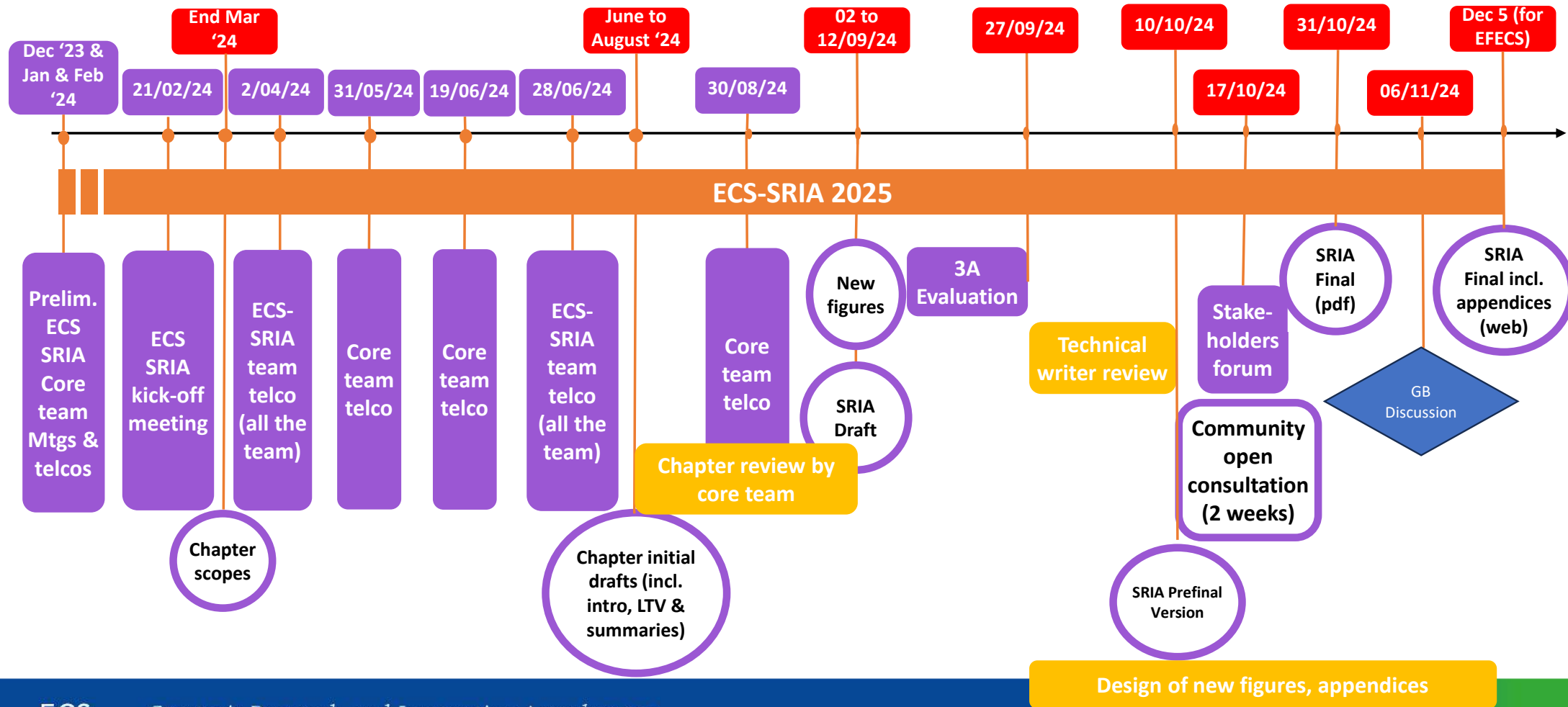
More than 280 European experts

- Interdisciplinary
- Across the whole ECS value chain
- Representing industry, RTO and academia
- 24 countries

Complemented by an open consultation

ECS SRIA 2025 Timeline

Target availability: End of previous year



Process improvement: ECS SRIA 2026 online open consultation (now closed)

ECS — Strategic Research and Innovation Agenda

Home ECS SRIA 2025 ECS SRIA 2024 ECS SRIA 2023 Change History Contributors

1 Foundational Technology Layers

Chapter 1.1 Chapter 1.2 Chapter 1.3 Chapter 1.4

1.1 Process Technology, Equipment, Materials And Manufacturing

Semiconductor process technology, equipment, materials and manufacturing form the foundation of the ECS value chain producing the chip and packaged chip-level building blocks for all digital applications. Nano- and microelectronics are key to achieving digital sovereignty in Europe, and therefore a range of solutions for a green and sustainable society. If Europe wants to control the development of a digital future fitted to its citizens and their requirements, as well as its social, economic, industrial and environmental goals, it needs continuous innovation in the field of semiconductor technology.

1.1.1 Scope

The key scope of this section is to cover all process technologies, equipment and materials' research and innovation to enable semiconductor IC manufacturing inside a cleanroom environment. This includes:

- New materials and engineered substrates to improve IC performance,
- Process technologies, equipment and manufacturing technology to advance integrated circuit (IC) functionality and/or systems on chips,
- Wafer level integration addressing a technology of packaging a die while it is still on the undiced wafer or bonded (attached to a wafer (DZW)). Protective layers and electrical connections are added to the substrate before dicing.

Clearly, the scope of this section as indicated in figure 1.1.1 below involves synergies with other sections in this ECS-SRIA. First and foremost, the section links with Components, Modules and System Integration in Chapter 1.2. In addition, this section also links with Embedded Software and System of Systems (SoS) to allow for an integral system technology co-optimisation approach to deliver application-driven solutions. More details about the synergies with other sections are described in Sub-section 1.1.6.

Process Technology, Equipment, Materials & Manufacturing

Wafer manufacturing

3DIC

Package

Board / system

Compute & memory

Advanced functionality
e.g. sensor, actuation and other devices that enable advanced functionality

Advanced integration
e.g. 2.5/3D integrated devices, wafer-to-wafer, die-to-die

Packaged single chip

More Moore

More than Moore

Board / laminate

BGA

leadless

Packaged SoC

(Systems of) / Complex Systems

Key Application Areas

MOBILITY

ENERGY

INDUSTRY

Submit Your Feedback

Feedback submission opens on April 1, 2025.

We appreciate your feedback. Click the button below to open the form.

Open Feedback Form

Other AENEAS activities relevant for EU-Taiwan cooperation

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1 – International Cooperation on Semiconductors

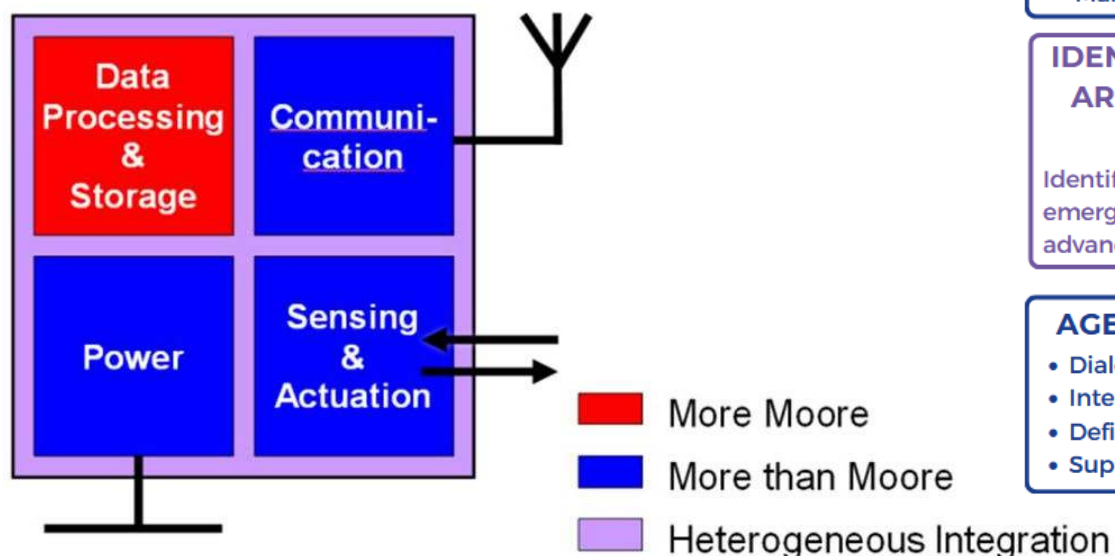


- Coordination and Support Action, Jan 2023 – Feb 2026
- Provide advice to the European Commission and support actions with the aim
 - To identify and support the establishment of the most promising scientific international collaborations
 - To build balanced semiconductor partnerships with like-minded countries
 - To set out cooperative framework on initiatives of mutual interest
 - To strengthen Europe's and partner Country's positions in global value chains in this area and to contribute to the EU Chips Act, Green deal and Digital Agenda



Scientific Coverage & General Approach

- Advanced computing & Advanced functionalities: sensing, RF & optical communications, optical devices, energy harvesting, power devices, ...



IMPLEMENTATION

EXHAUSTIVE ANALYSIS OF SEMICONDUCTORS' VALUE CHAINS, FOR ELECTRONICS & PHOTONICS

Identification of :

- EU's economic and industrial strengths & weaknesses
- Strategic dependencies
- Market and cooperation opportunities

IDENTIFICATION OF RESEARCH AREAS FOR INTERNATIONAL COOPERATION

Identification of next generation & emerging technologies, especially in advanced computation and functionalities.

DETERMINATION OF MOST INTERESTING COUNTRIES FOR INTERNATIONAL COOPERATION

Identification of challenges for which international cooperation is critically important.

AGENDA FOR AND INITIATION OF INTERNATIONAL COOPERATIONS

- Dialogue with actors of existing cooperation
- International collaboration with non-EU national authorities
- Define standardisation needs and activities
- Support the European Commission

Geographical coverage





Semiconductor Ecosystem TAIWAN

Main Stakeholders

POLICYMAKING

1. Ministry of Economic Affairs (MOEA)
2. Department of Industrial Technology (DOIT) under the MOEA
3. National Science and Technology Council (NSTC)

RESEARCH ORGANISATIONS

1. Industrial Technology Research Institute (ITRI)
2. National Applied Research Labs (NARLabs), incl. Taiwan Semiconductor Research Institute (TSRI)

INDUSTRY ASSOCIATIONS

1. Taiwan Semiconductor Industry Association (TSIA)
2. SEMI Taiwan

INDUSTRY (NON-EXHAUSTIVE)

3. ASE Technology Holding (Assembly & test, world's top provider)
4. GlobalWafers (Materials, silicon wafer supplier)
5. MediaTek (Fabless IC Design, largest Taiwanese design house)



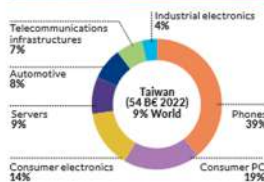
6. Nanya Technology (Memory, DRAM producer)
7. PSMC - Powerchip Semiconductor Manufacturing Corporation (Memory, foundry services)
8. Realtek Semiconductor Corporation (Fabless IC design, networking and multimedia chips)
9. TSMC (Foundry, world leader in contract chip manufacturing)
10. UMC (Foundry, major contract manufacturer)
11. VIS - Vanguard International Semiconductor Corporation (Specialty IC foundry)

Funding Instruments

- Statute for Industrial Innovation ("Taiwan Chip Act", amended 2023): 25% R&D tax deduction, 5% CapEx deduction (advanced processes); no fixed budget, incentives provided via tax deductions; Ministry of Finance (Art. 10-2, Statute for Industrial Innovation) [3].
- Chip-based Industrial Innovation Program: NT\$300 billion (~€9.3 billion) (2024-2033) for industry-academia collaboration, AI chip R&D, infrastructure development [1].
- NSTC Annual Tech: Budget NT\$159.5 billion (~€4.9 billion) (2024), proposed NT\$180 billion

- (~€5.6 billion) (2025): Funds allocated to semiconductor ecosystem enhancement ("Chips Team Taiwan" initiative) [2].
- Talent Cultivation Act (2021): Legal basis for university-industry R&D and semiconductor workforce expansion [2].
- NSTC Talent Program: NT\$35 billion (~€1.1 billion) to fund scholarships and hands-on training (~2,100 chip experts/year) [2].
- Science Park and Foreign Investment Incentives: Tax benefits, subsidies, and infrastructure for domestic and foreign semiconductor investors.

Demand by Application



The distribution is the average for South-East Asia.
Source: DECISION Bytes & Conseil

Market and Production Share



Outcomes

• Reports

- Economic analysis
- Analysis of EU-international cooperation
- Future technologies in advanced computation
- Future technologies for advanced functionality
- Recommendations for International Research Cooperation

• Factsheets

• Joint workshops

- So far Japan, South Korea, Singapore

• Joint Chips JU calls

- South Korea, Japan
- Taiwan under discussion for 2026

- <https://icos-semiconductors.eu/other-outcomes/factsheets/>
- <https://icos-semiconductors.eu/public-deliverables/>
- <https://icos-semiconductors.eu/>

Possible Joint activities

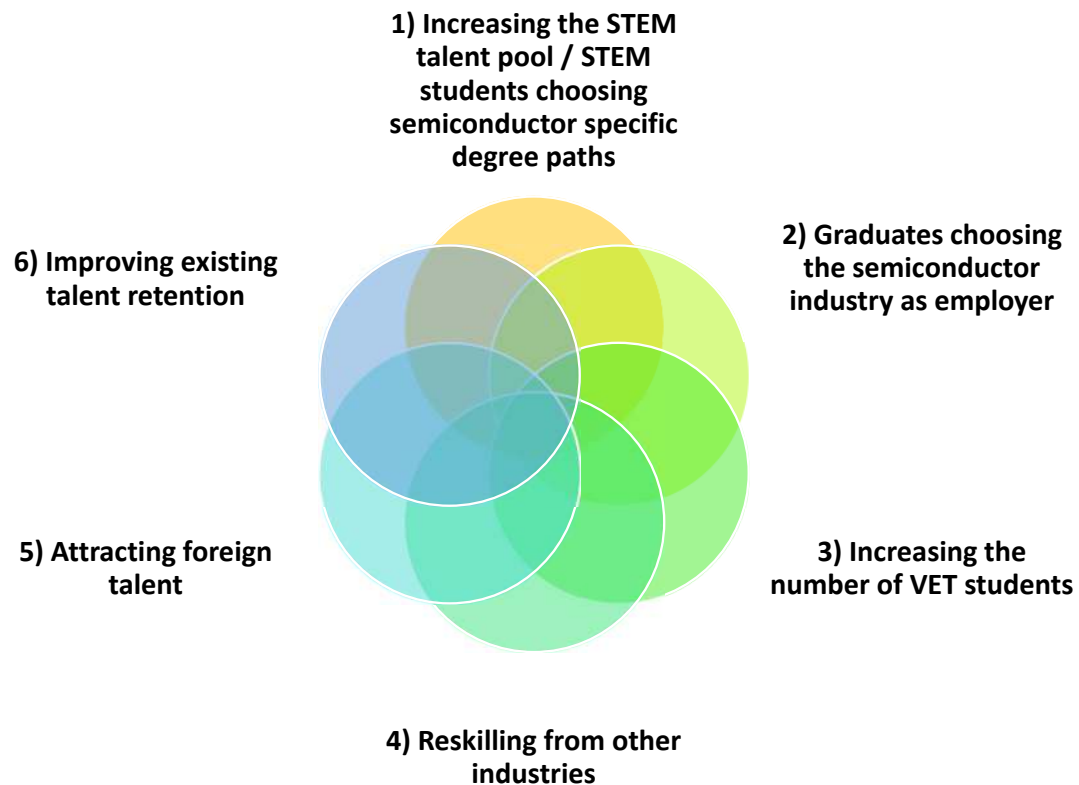
- **Webinars**
- **Workshops**
- **Contribution to Regional & International Technology Roadmaps (IRDS)**
- **International R&D&I cooperation on topics of mutual interests**
- **Exchange of researchers**
- **Access to Research Infrastructures**
- **Standardisation needs for emerging technologies**

Other AENEAS activities relevant for EU-Taiwan cooperation

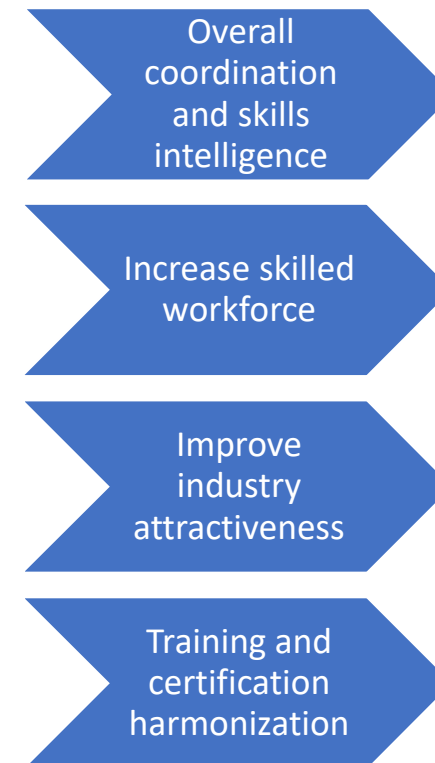
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2 – Tackling the talent gap

Talent Gap To Be Tackled Via Many Angles



- **Potential areas for cooperation on skills**



Opportunities for collaboration between Taiwan and Europe

Where can AENEAS help?

- Collaborative international R&I projects
 - Xecs
- Identifying topics of common interest
 - Investigate joint workshop Chips JU / Taiwan
- Researcher mobility
- Tackling the talent gap
 - Sharing best practices
 - Joint actions



Thank you

For more information
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